Nanomanufacturing in Semiconductor Microelectronics

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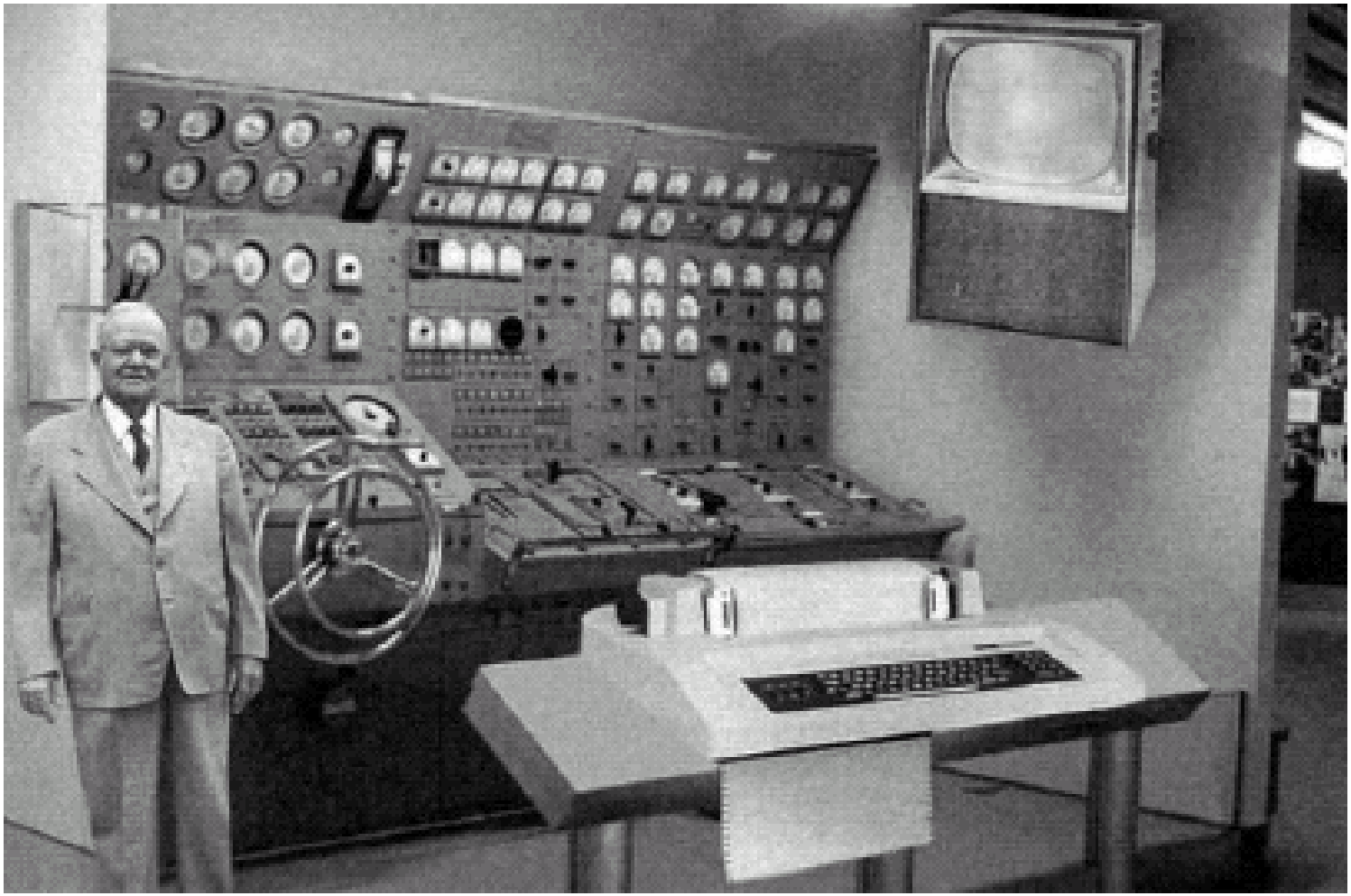
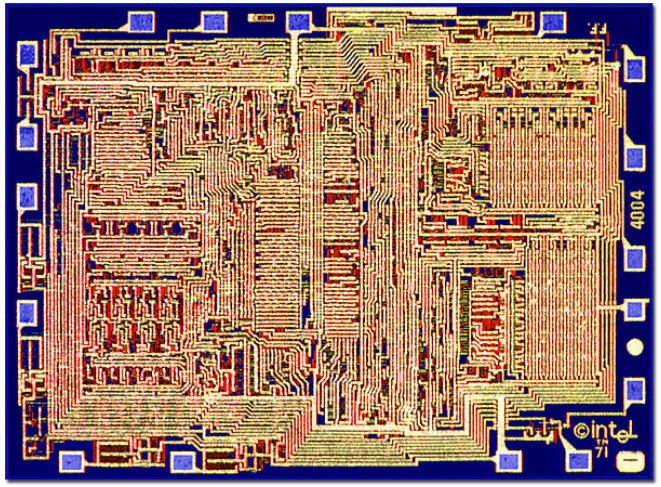
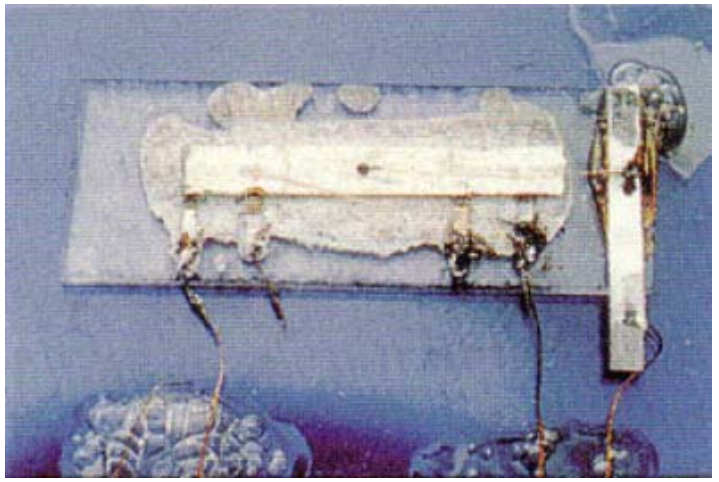
In 1954, a popular magazine asked "What would a home computer look like 50 years later, in 2004. Remember, there were very few computers of any kind at this time.



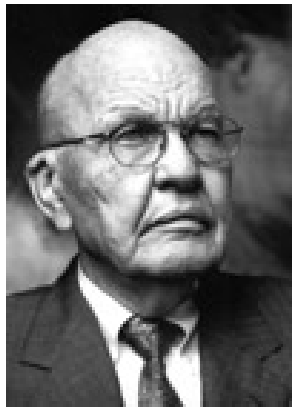
The new technology that revolutionized the computer, and the entire information processing world, was the creation by Texas Instruments and Intel of the microprocessor.



Intel 4004 microprocessor



T.I.s first integrated circuit



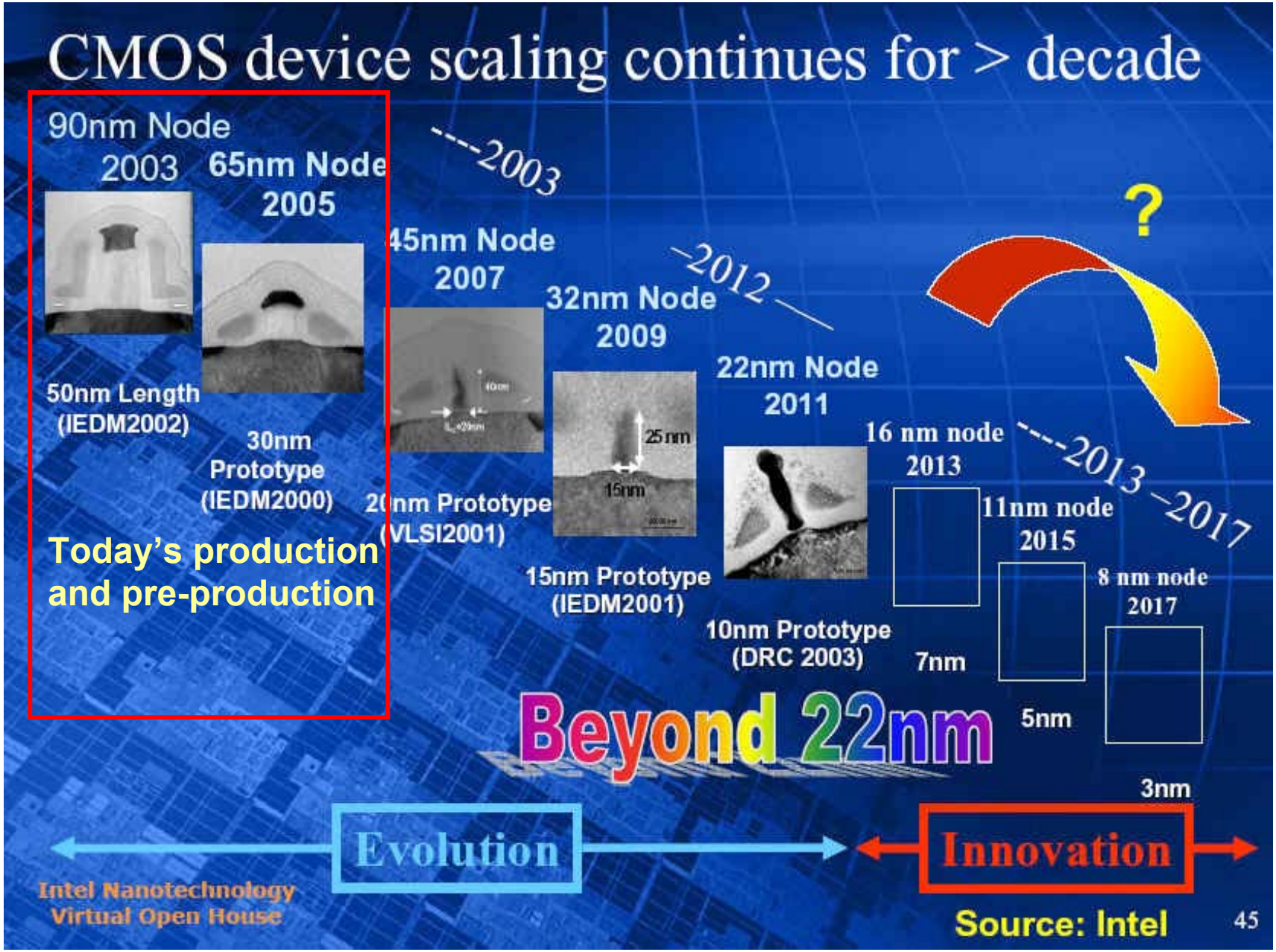
Jack St. Clair Kilby
Nobel Prize 2000
Invention of the integrated circuit

As integrated circuits became more dense and had smaller feature sizes, it was already clear that manufacturing was a problem:

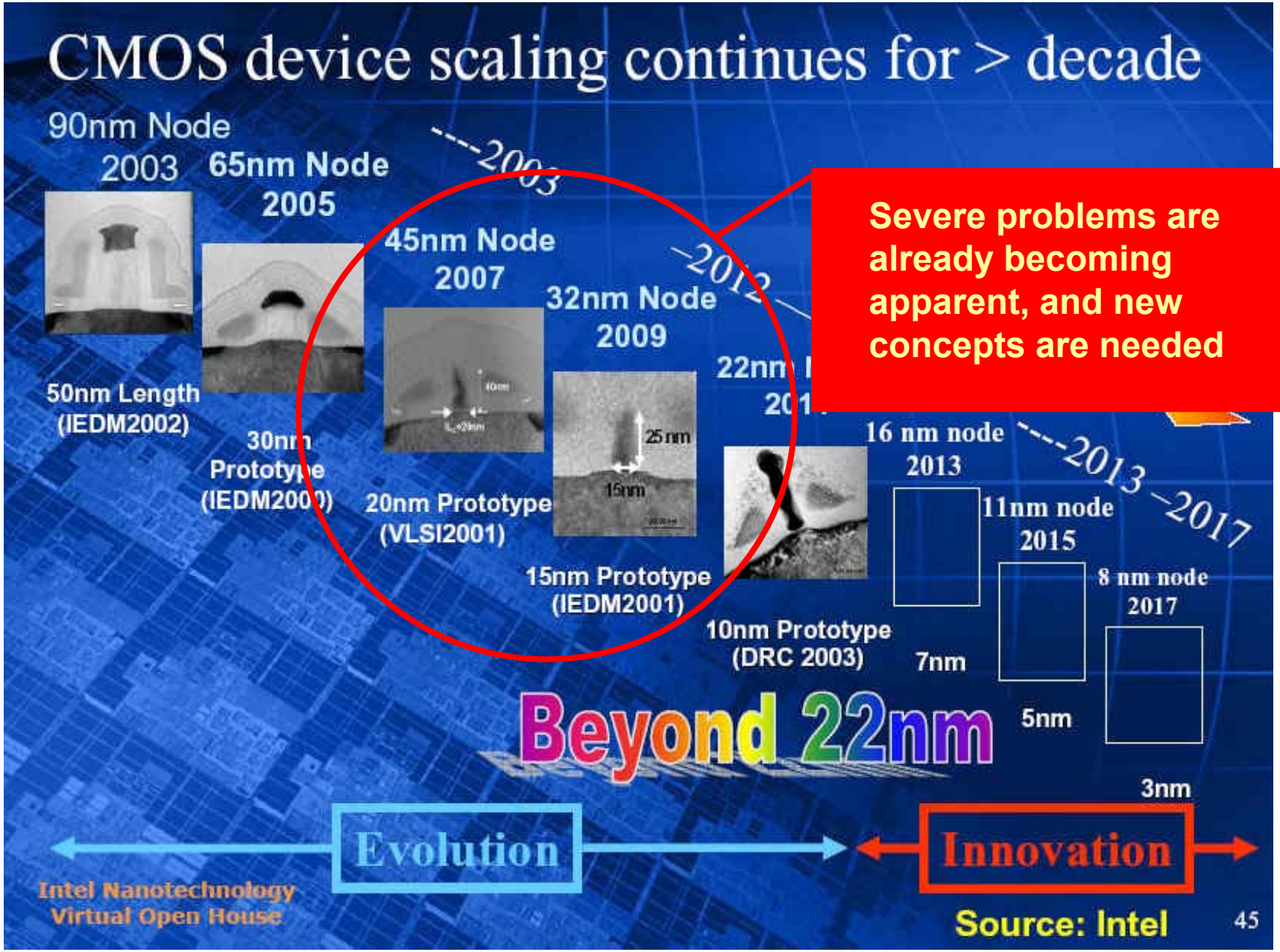
> "…fabrication methods are limited by the general uncertainty relation, by scattering or by minimum size of photoresist molecules, …considerations of statistical doping fluctuations, …increases the minimum (feature) size to about 10 μm for a very complex (10^5 elements) circuit…"
>
> J. T. Wallmark, Inst. Phys. Conf. Ser. 25, 133 (1975).

Indeed, reduction in the *theoretical* minimum feature size has barely kept ahead of the research chips!

CMOS device scaling continues for > decade



CMOS device scaling continues for > decade



Severe problems are already becoming apparent, and new concepts are needed

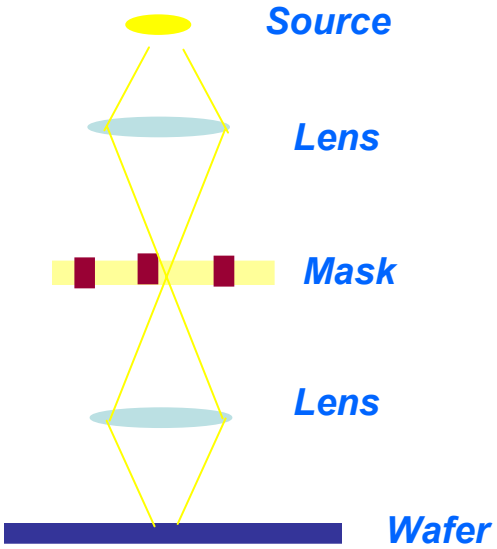
P. Gardini, Intel

Manufacturing in the Si semiconductor industry is based upon one key technology, and that is the process of *lithography and pattern transfer*.

Lithography is essentially a photographic process, in which a pattern present in a mask is transferred to a photosensive material (the photo-resist) on the surface of the wafer.

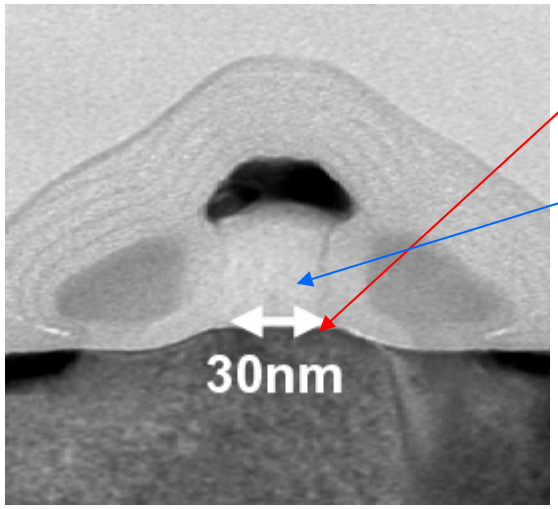
This process is carried out by machines called "steppers" as they step across the wafer doing multiple exposures.

As much as 70% of the cost of a fab is lithography tools!



This process has several key steps, any one of which can limit the ability to continue to effectively manufacture future generations of chips.

- The light source
- Photoresist material
- Alignment of multiple levels in the process
- plus…

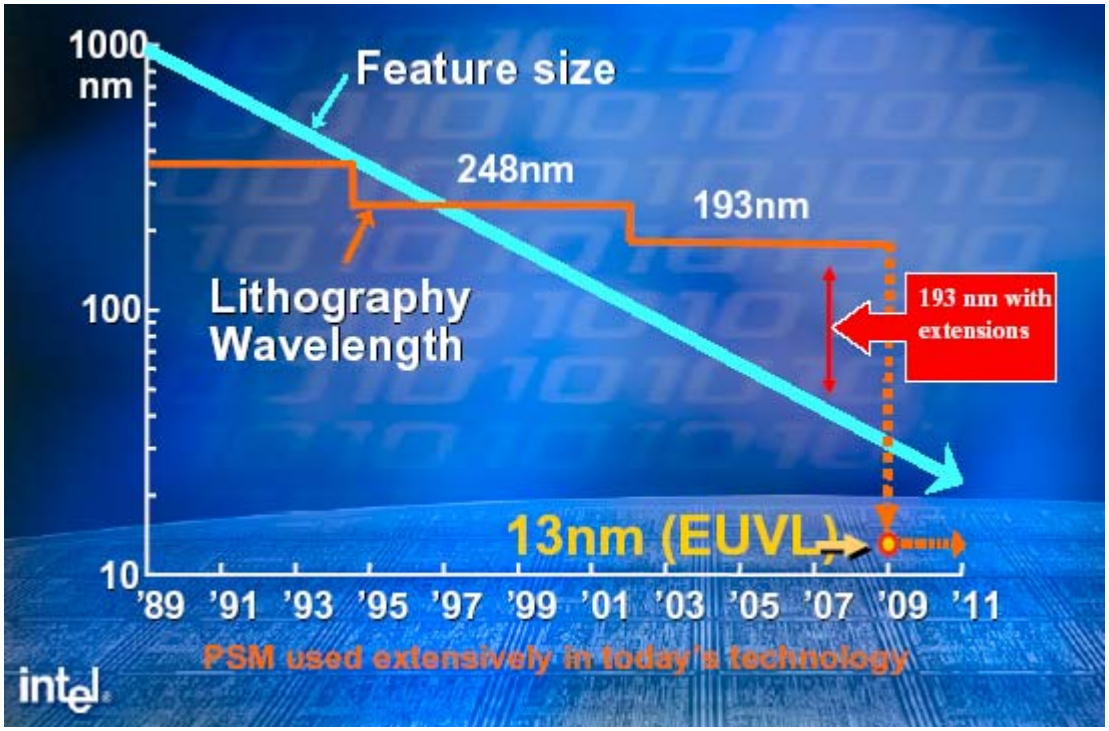


Growth of 1 nm thick oxide must be uniform across 300 mm wafer

Alignment of the gate material must be to within 1-3 nm across the entire 300 mm wafer. Eased by self-aligned processes, but then position of source and drain become the critical alignment.

As we move beyond critical dimensions of 30 nm in today's devices, new exposure tools will be required—use of 193 nm wave length light in air will no longer produce the resolution required.

One new approach is with Extreme Ultra-Violet (EUV) with 13.5 nm wavelength.



Ken David, Intel,
ftp://download.intel.com/research/silicon/EUV_Press_Foils_080204.pdf

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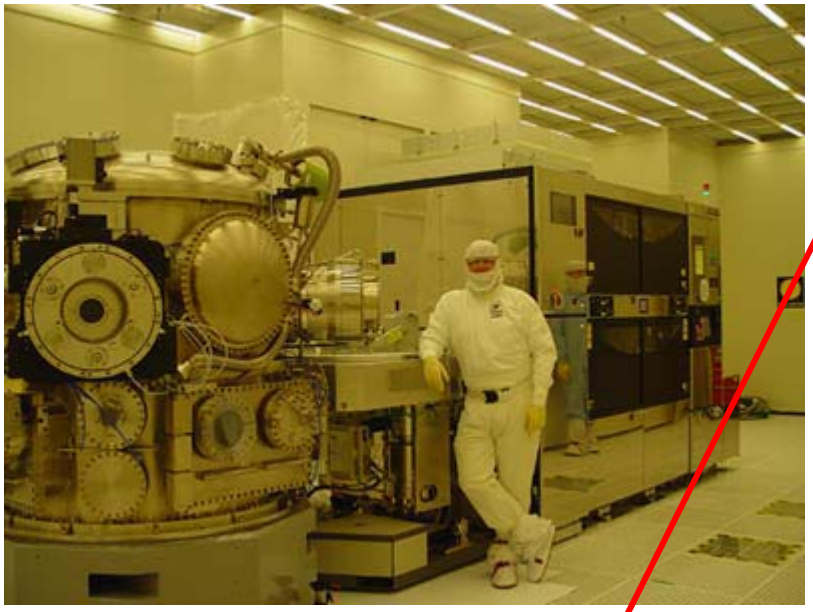
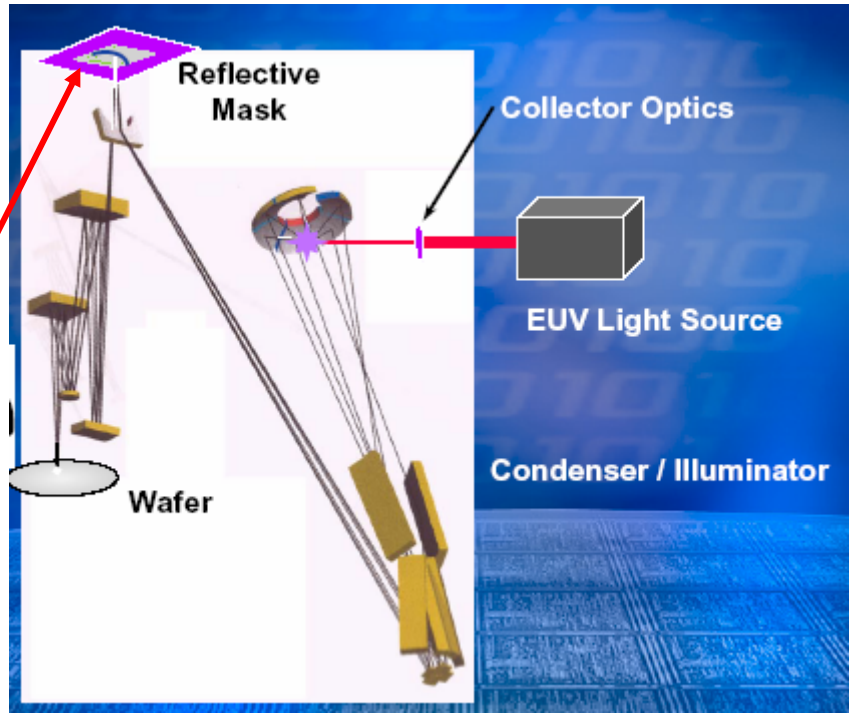
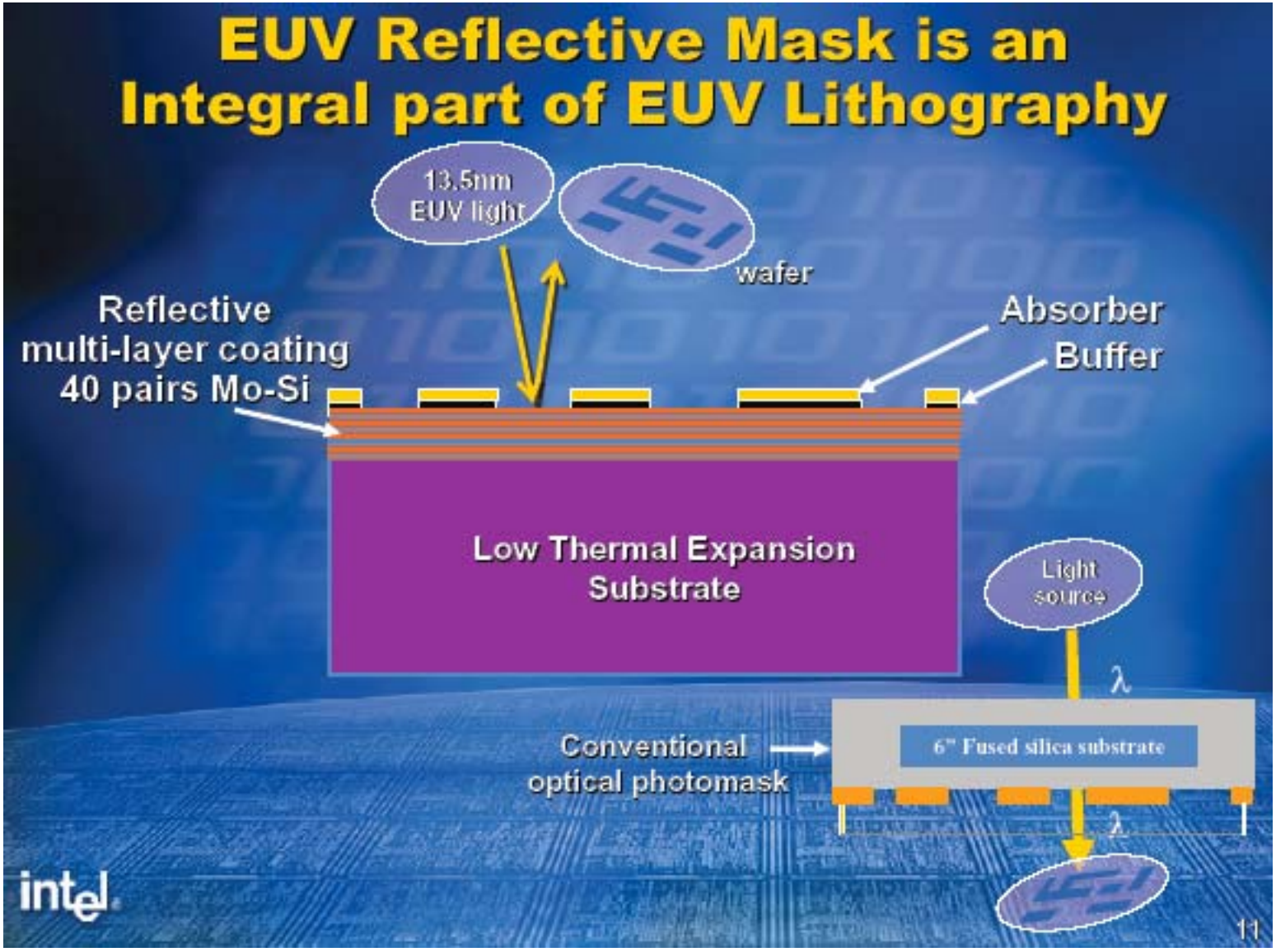


Intel's Micro-Exposure Tool (MET) for EUV lithography development



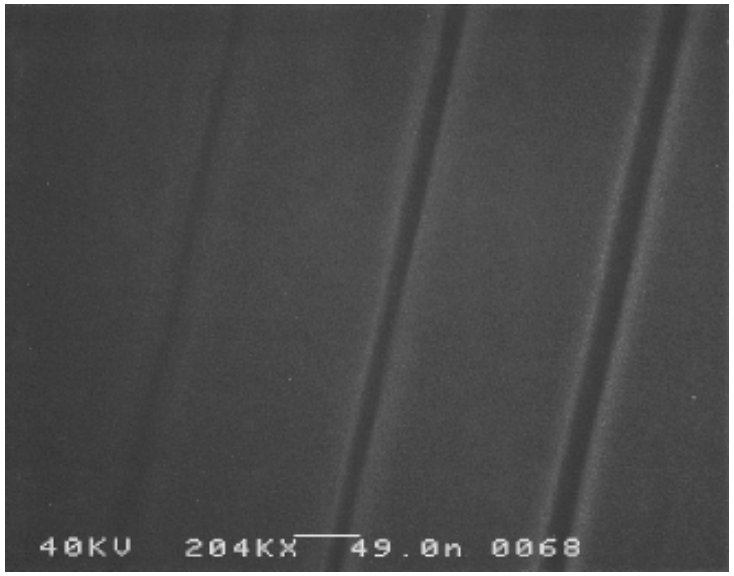
But this requires a new mask technology, since reflection masks must be used.

(Current masks are transmission masks.)



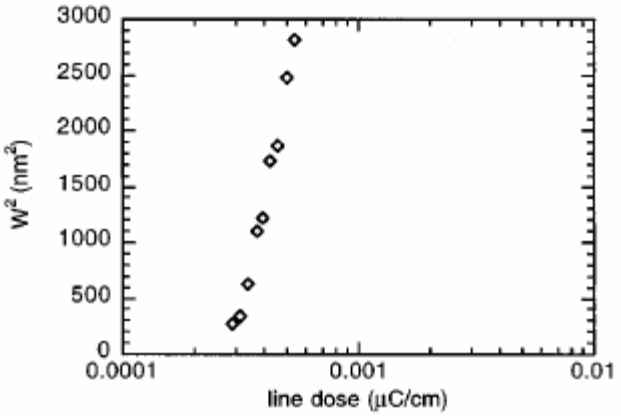
Ken David, Intel, ftp://download.intel.com/research/silicon/EUV_Press_Foils_080204.pdf

We also need to develop new or improved resists, as resist development is definitely hindered by exposure tool resolution and by process variability. We need both: *better resolution and controlled processing*.



M. Khoury and D. K. Ferry, JVST B 14, 75 (1996).

Small lines (≥6 nm) obtained in PMMA



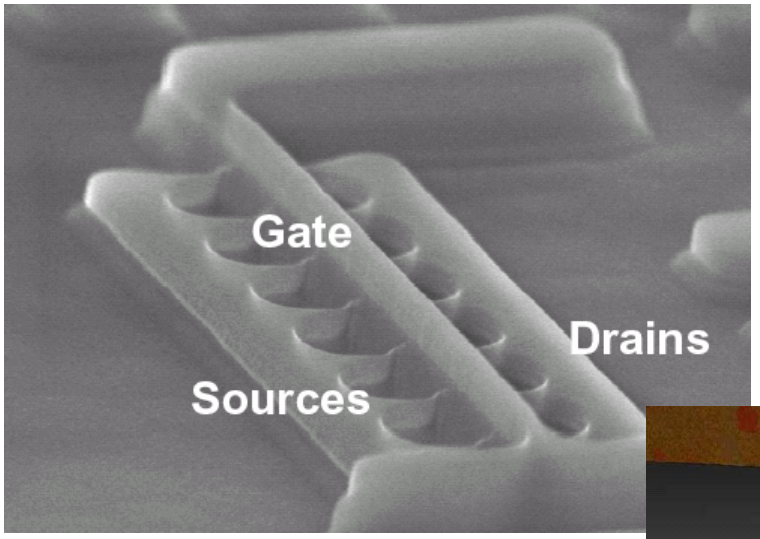
But, PMMA (the highest resolution resist) is generally thought to be too slow for industrial use.

At ASU, we are also pursuing studies of ZEP-520, a faster high resolution resist, in our JEOL 6000 e-beam system for ultra-high resolution (approaching that of PMMA).

This resist should also be usable by EUV tools.

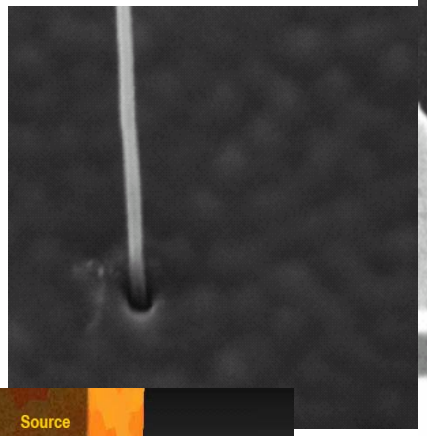
The process of nanofabrication is expected to get much more detailed in coming years. *This is not just because of reduced dimensions and constraints on lithography*.

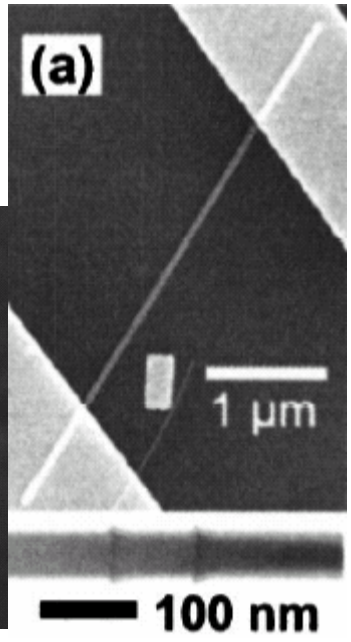
Device structures will get more complicated.

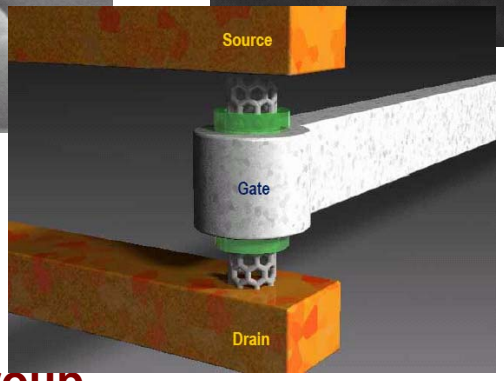


Intel Tri-gate structure
R. Chau, Intel

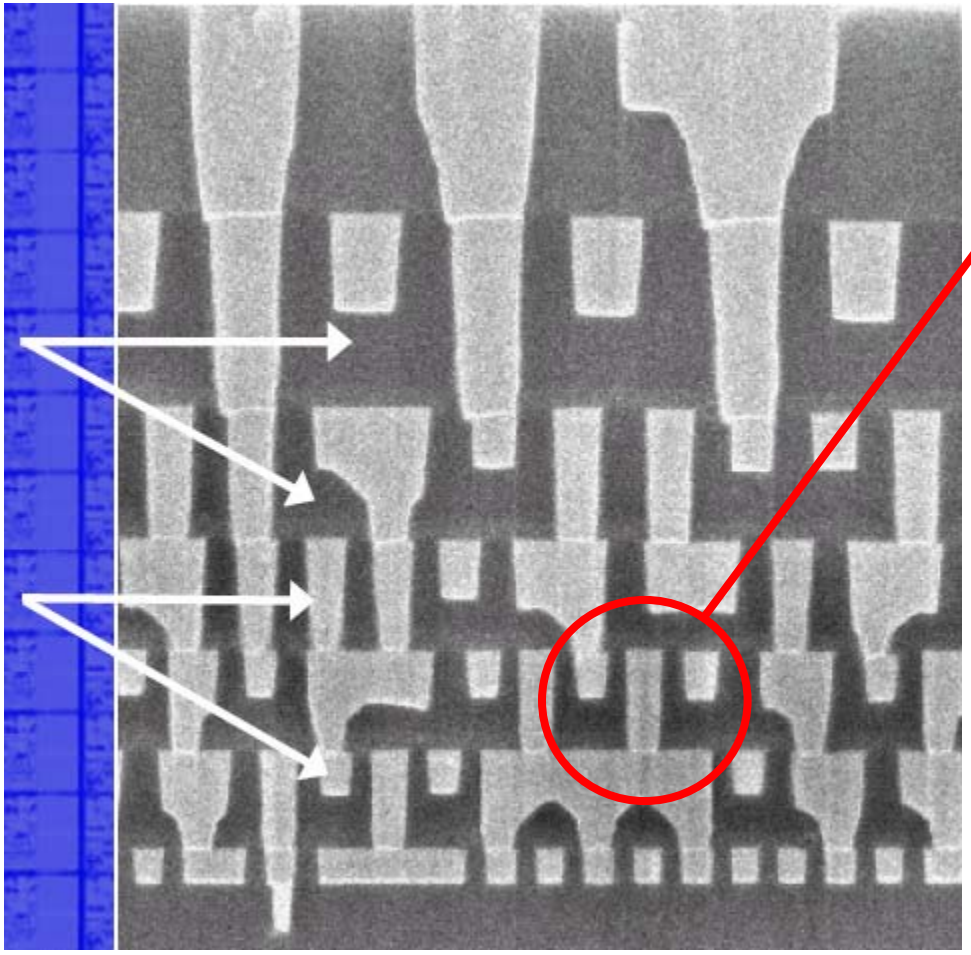
Semiconductor nanowires







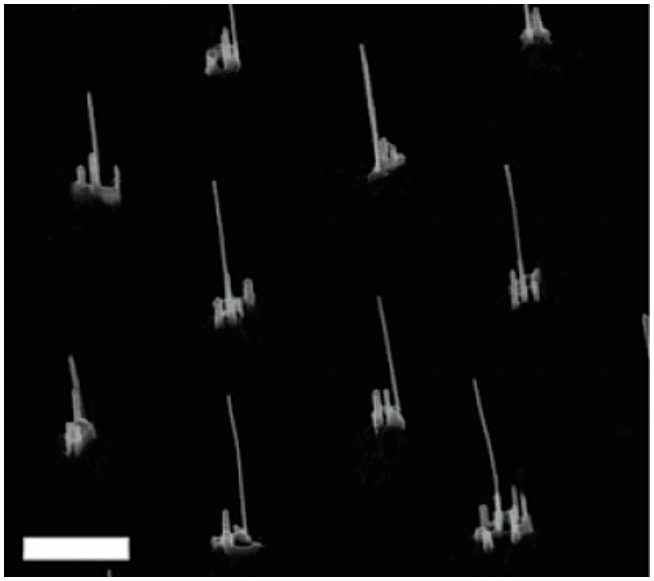
Gated vertical CNT concept (Siemens)

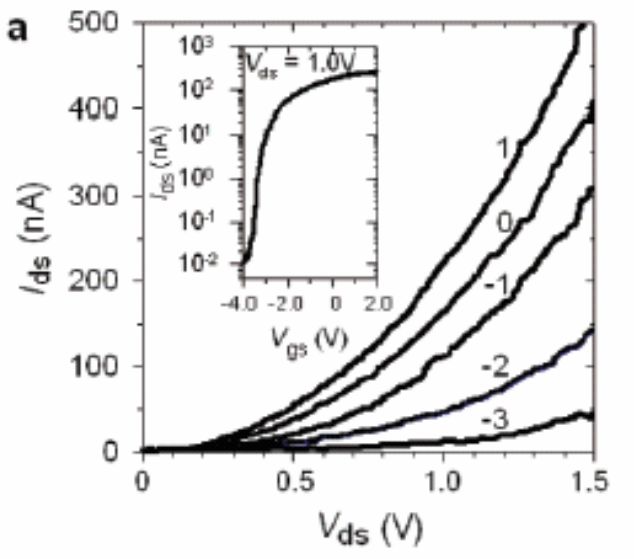


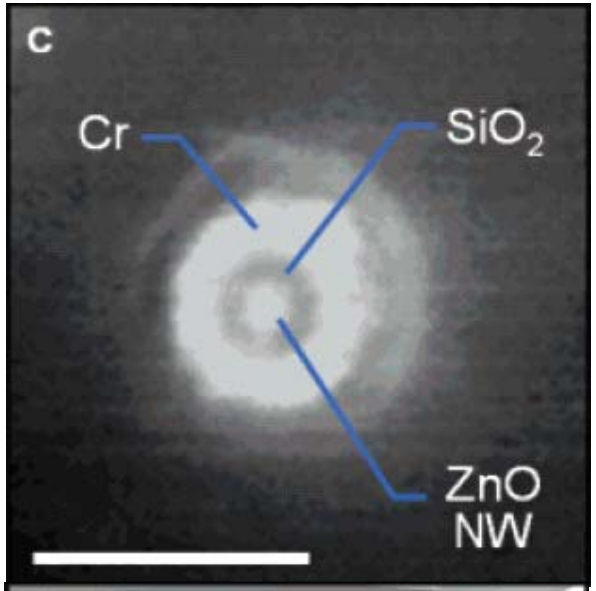
Cross-section of Intel Pentium metallization layers.

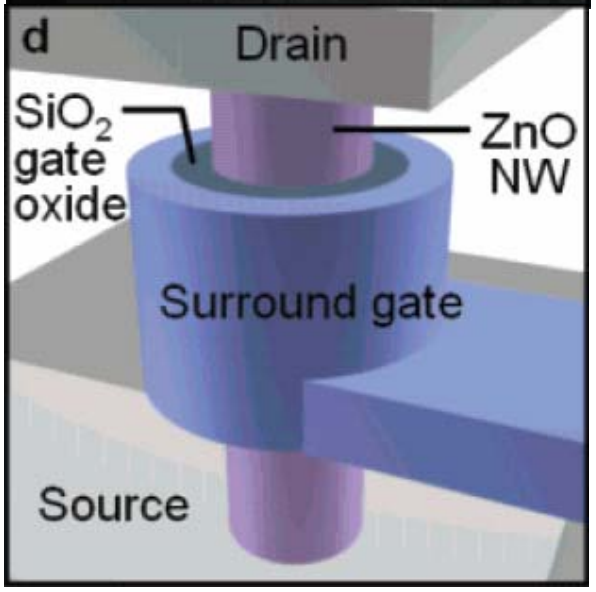
The idea of using vertical devices, either at the Si surface, or in the interconnect layers, opens the door to novel new reconfigurable logic circuits.

ZnO Nanowire MOS Transistors

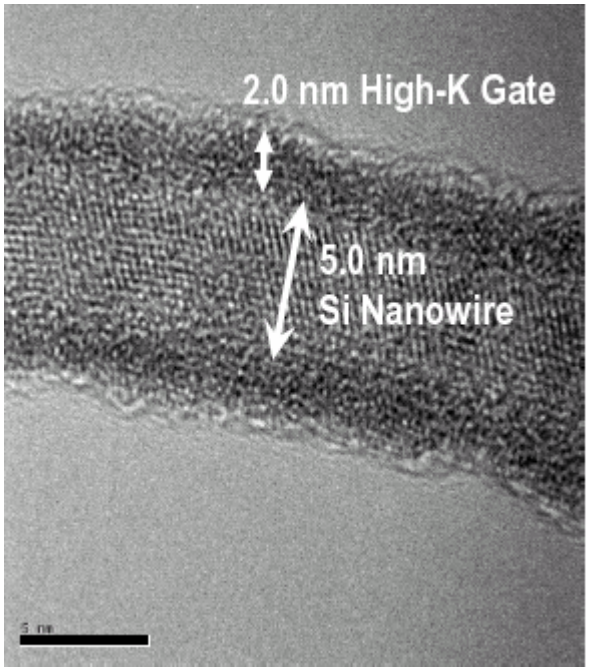






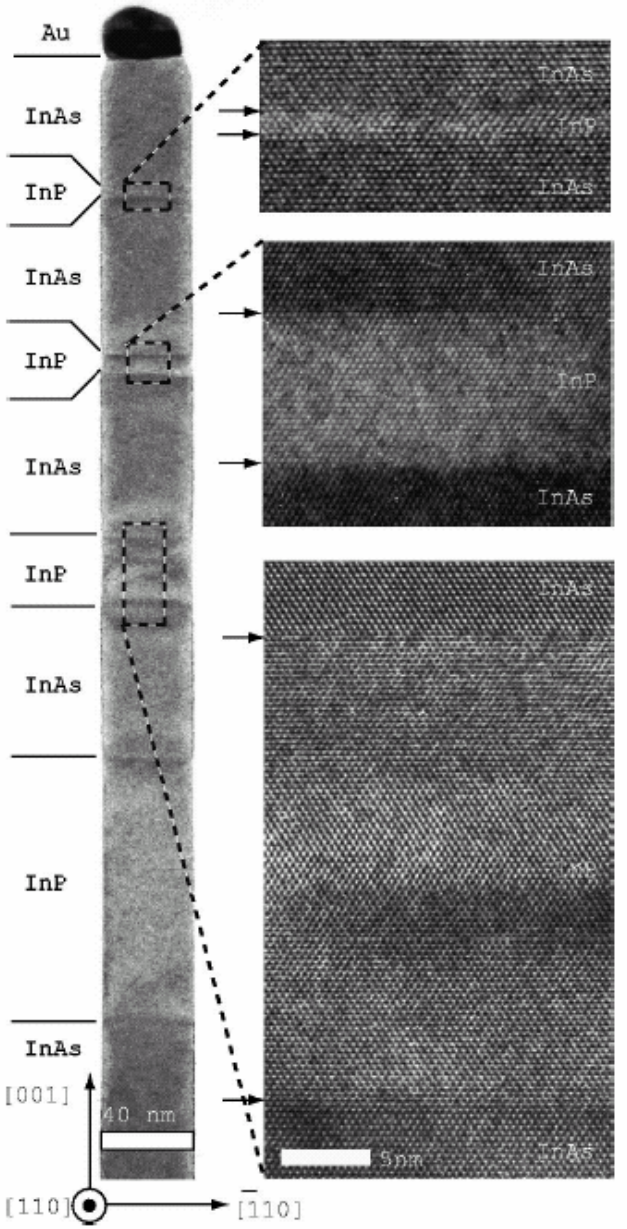


Ng *et al.*, Nanolett. 4, 1247 (2004).



Intel Si MOS nanowire device
R. Chau, Intel

InAs based heterostructure wisker tunneling device



Björk et al., Appl. Phys. Lett. 80, 1058 (2002)

One important question is: Will device operation change at these small sizes? That is, will the physics of the device limit how small we can make transistors?

This question has been addressed for as many decades as we have been making integrated circuits.

As pointed out earlier, the theoretical limiting size has been going down continuously with the device scaling.

Can we address this question in a better manner?

Semi-classical modeling of semiconductor devices has proceeded to where we have very efficient ensemble Monte Carlo techniques which can investigate detailed many-body effects in small devices, as well as surface-roughness, discrete doping, random potentials, etc.

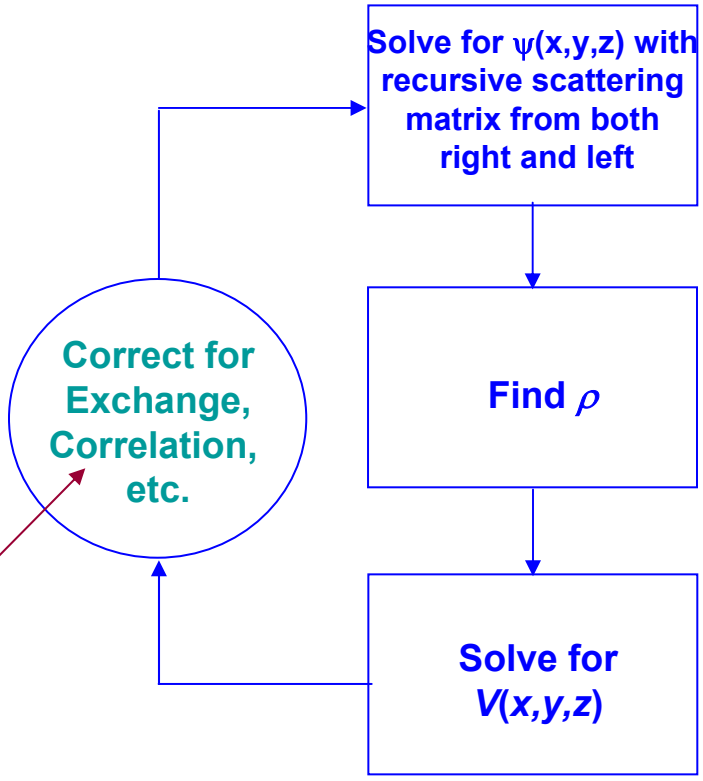
On the other hand, device down-scaling is approaching a size which is comparable to the carrier coherence length, and within an order of magnitude or so of the de Broglie thermal wavelength.

Many approximate techniques for first-order quantum corrections have been proposed: density gradient, effective potential, etc. These are not adequate on this size scale.

This means that new, fully quantum mechanical approaches are needed to study the coherent quantum behavior in these devices.

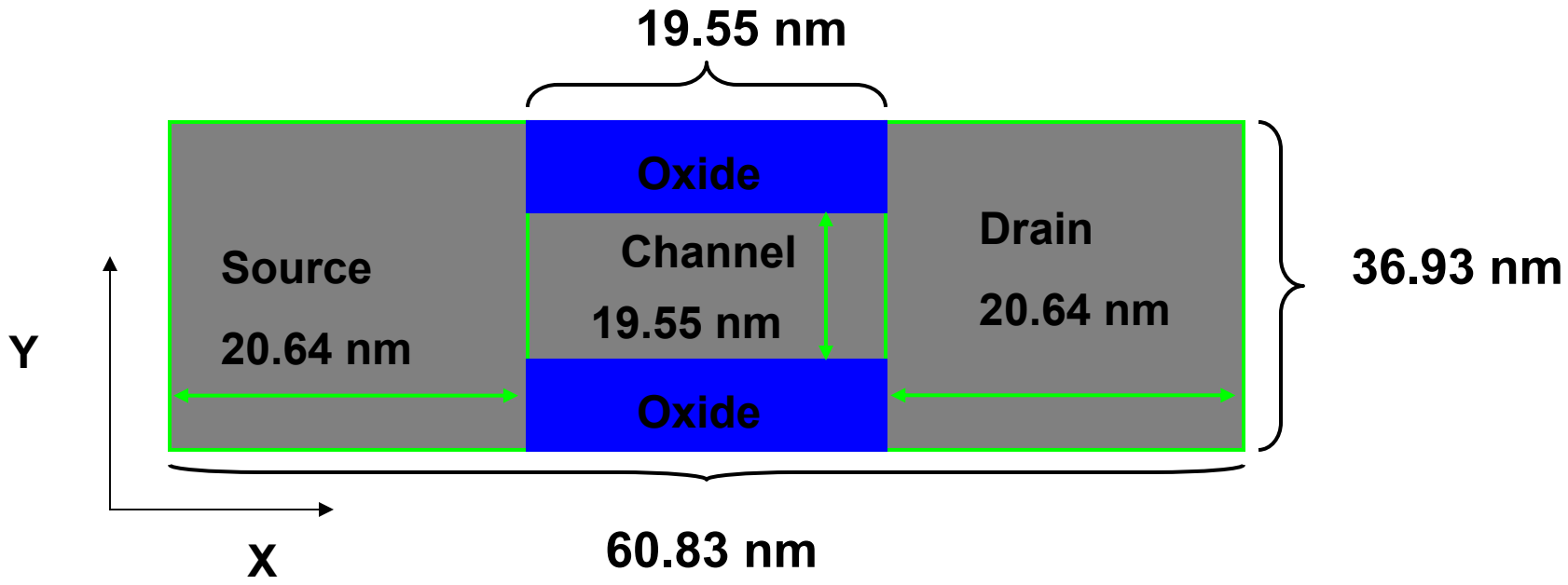
Ours is not the first such simulation, and others have used direct solutions of the Schrödinger equation, Green's functions, quantum hydrodynamic equations, etc. We feel that our approach is better, and allows us to incorporate scattering effectively, while being more computationally efficient than e.g. Green's functions.

For our systems, we can generate a relatively straight-forward loop to find the solutions:

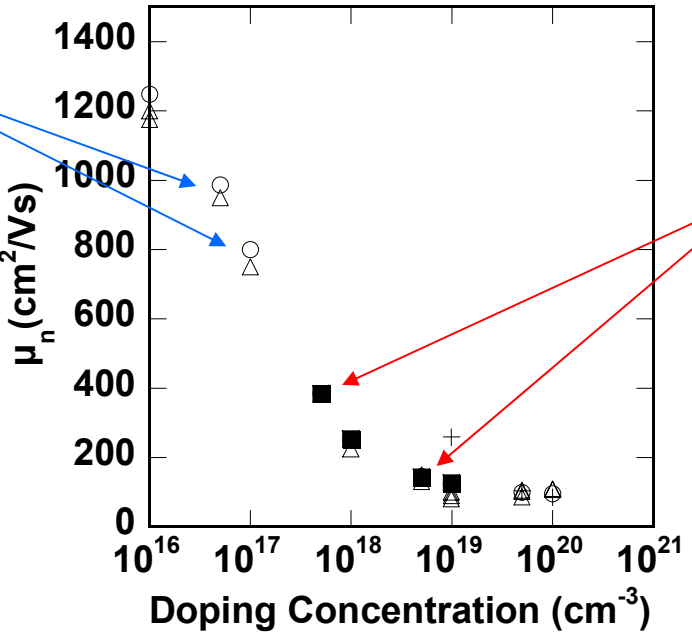


Often requires the Fermi energy to be adjusted to keep density constant.

We initially consider a relative large cross-section device, whose properties are nearly bulk-like. Impurities are considered exactly within the Poisson equation.

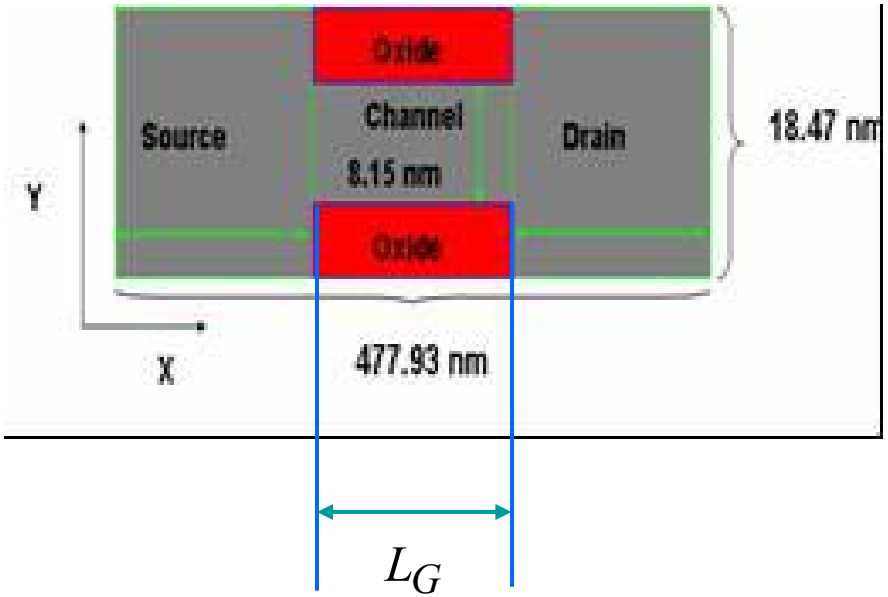


Open symbols are experimental results taken from the literature.



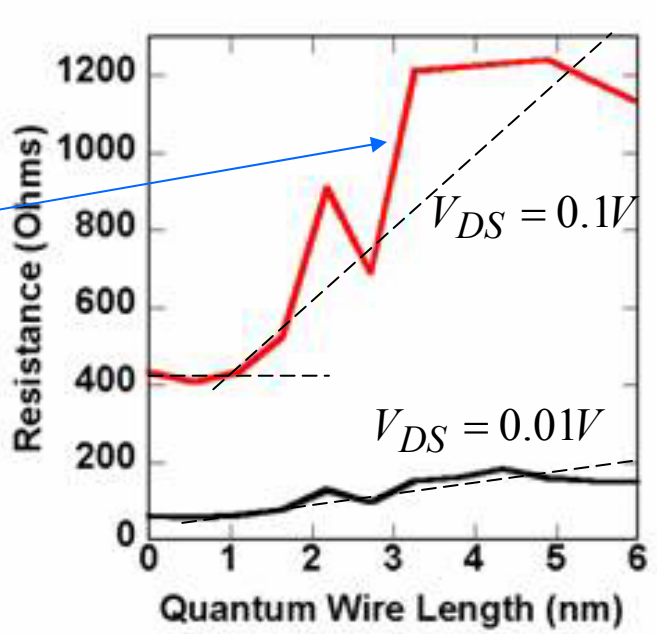
Closed symbols are the calculated mobility, limited by impurity and phonon scattering.

Then we go to a smaller device, and vary the channel length. For devices, in which phonon and impurity scattering dominate ballistic transport, the resistance will increase with the length of the channel.

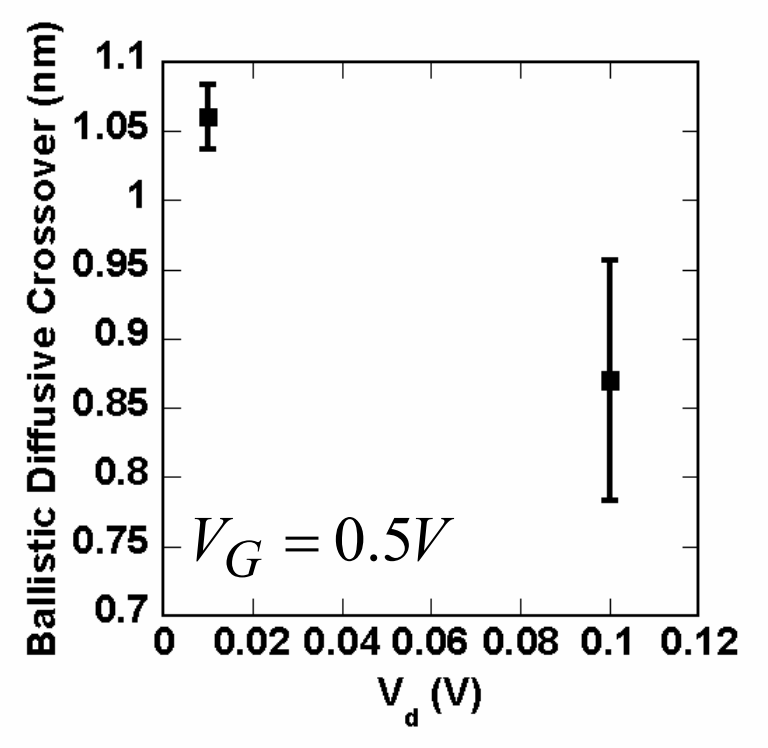


$$V_G = 0.5V$$

Fluctuations are due to quantum interference, even in the presence of scattering.



Devices will continue to operate as we expect them to down to gate lengths below 1 nm. However, there will be enhanced quantum interference effects, which will likely make device-to-device variations larger and must be designed for.



- Manufacturing is a major part of the *scaling* of integrated circuits to ever smaller dimensions.

- One key ingredient in integrated circuits is lithography, and new tools are continuing to be developed each year. The requirements, in terms of resolution and alignment, continue to become more exacting with parts per billion expected today and exponentially more exacting factors expected in the future.

- Nevertheless, we see no physical limitations on the performance of today's FETs for several generations into the future.